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PQM Gain Extension

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The decision of PQM gain bases on the optical fiber communication system receiver sensitivity of –32 dBm, after a 90:10 optical couple, the sensitivity is –42 dBm at which a PQM has the output voltage about 0.4 V that is enough for the normal operation of A/D converters and comparators.
If higher sensitivity is required, an extern amplifier is needed, which is shown in Fig.1.

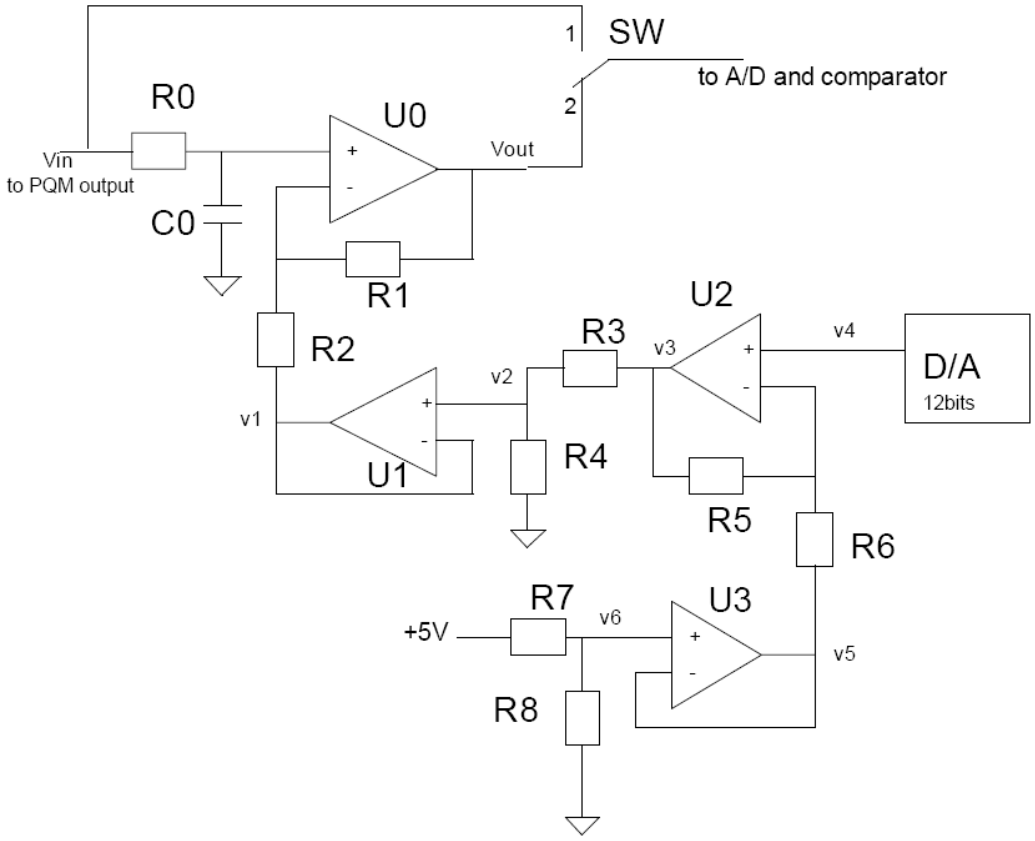

Fig.1

1. Circuit Description

The gain of the external amplifier can be set from 2 to 500, in the following description, the gain of 500 is assumed, for other gains, the part values can be

calculated from the formulas provided.

In Fig. A4-1, U0, U1, U2 and U3 are high stable, low input offset operational amplifiers, such as Linear Tech LTC1047.

All the operational amplifiers should operate the power supply voltages of +5 V and –5V.

U0 is the main amplifier, U1 and U3 are voltage followers which convert the impedance. U2 is a voltage shifter.

When the switch SW is set to position 1, the PQM output is connected to A/D and comparator directly, the amplifier is by passed. When the switch is set to position 2, the amplifier is in the signal chain and the system gain is increased

The Vishay DG series analog switches such as GD2001 are recommended for SW
U0 is the main amplifier and its gain depends on the ratio of R1 and R2.

Since the PQM has dark voltage which ranges from –50mV to +50mV, it is necessary to have a dark voltage cancellation voltage v1..
Vout =(1+R1/R2)Vin – (R1/R2)v1 (1)

The factor of (1+R1/R2) is the gain, usually R1 can be as large as 1 Mohms for the gain of 500, R2 is 4.99 K ohms.

When the gain is 500 without the dark voltage cancellation, U0 output voltage could be +25V or –25V, far exceeding the power supply voltage. Therefore the dark voltage cancellation is absolutely necessary.

When the dark voltage cancellation is considered, set Vin to zero,

‘v1 = Vout/(R1/R2) (2)
R1/R2=500

Vout ranges from –50mV to +50mV, v1 should cover the range from ‑ 0.1mV to 0.1 mV at least. But the real coverage of v1 should be ten times of the minimum range, that means from –1mV to +1 mV.

The dark voltage varies over the temperature variation and PQM gain settings. The external amplifier is used at the PQM gain setting of G4, the highest gain, therefore the temperature variation of v1 should be considered only. Since temperature would change during PQM operation, proper values of v1 should be pre measured, saved in

an non volatile memory.

The voltage of v1 sources from the output voltage v4 of the digital to analog (D/A). D/A with the resolution of 12 bits and the output voltage range of 0 to 2.5V is recommended.

In the voltage shift circuit, R5=R6=100 K ohms,
‘v3=2v4-v5 (3)

Set v5=v4=2.5V, when v4 varies from 0V to 2.5V, U2 output v3 is changed from –2.5V to +2.5V.

R3 and R4 form a voltage divider which mapps v3 coverage of –2.5V to +2.5v to the range of –1mV to +1mV by R3 of 250K ohms and R4 of 100 ohms

R7, R8 and U3 generate the shift voltage of v5,

The voltages of v5 and v6 are the input and output of the voltage followers U3,
‘v5=v6

Set R1=R2=100 K ohms, v6=2.5V

2. Calibration Operation

During the system calibration, one more procedure should be added, that is the dark voltage cancellation.
1) No any light enter the PQM
2) Set the switch to Position 2
3) Set the PQM gain to G4, the largest gain.
4) Set a temperature
5) Start A/D and sample the data of Vout, sweep the D/A code to find the code which set U0 output to about 100 mV, then sample Vout 1000 times, calculate the average value, Vout_b. In the high gain system, the noise with power supply frequency 50/60Hz would appear in the output voltage, if it is the case, let the sample time should last over several period of the power supply frequency cycles.
6) Save the code and the value of Vout_b with the temperature in the non volatile memory.
7) Set to next temperature, usually take the temperature step of 1C
8) Repeat 4) to 6) until all the operation temperature range is covered.

3. Normal Operation

During normal operation, when the high sensitivity is required, turn the switch to Position 2, before A/D operation, read the temperature, then set the D/A code according to the temperature. Sample Vout 1000 times, average the sampled data to get mean value of Vout_m, the effective output voltage Vout_e =Vout_m-Vout_b.

4. A/D and voltage comparator selection

The voltage values at different gain of the external amplifier, the input optical power at PQM G4 of 5000 V/mW are listed in Table 1

	Gain of 10	Gain of 50	Gain of 100	Gain of 500
-60 dBm	0.05V	0.25V	0.5V	5V
-70 dBm	0.005V	0.025V	0.05V	0.5V
-80 dBm	0.0005V	0.0025V	0.005V	0.05V

Table 1

It is obvious that high resolution A/D must be used for the weak optical power measurement.

Table 2 shows the voltage resolutions of different A/D bit number at the reference voltage of 5 V. From the table, A/Ds with 16 bits or more are recommended.

A/D bits	Voltage resolution	A/D bits	Voltage resolution
8	19.5mV	18	19.1uV
10	4.88mV	20	4.77uV
12	1.22mV	24	0.398uV
16	76.3uV		

Table 2

Since the output voltage Vout is very small, the voltage comparator must have very low input offset voltage of micro voltage order. If Vout is noisy, the comparator output would toggle which will cause a lot false interrupt and disturb the micro controller

normal operation. If in the case, the comparator output must be disable to the interrupt line and the software warning threshold is used instead.

A comparator output disable circuit is shown in Fig. 2

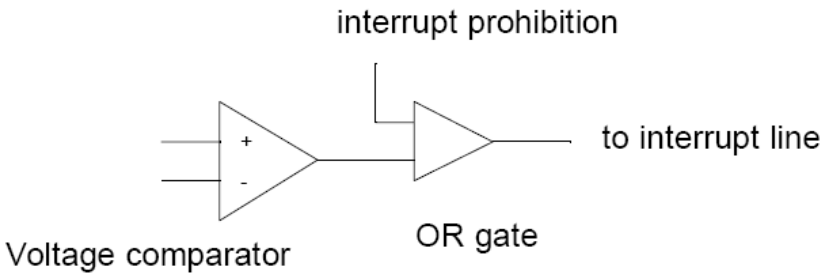

Fig.2.

Usually a transition from logic high to logic low on the interrupt line invokes a controller interrupt. When an active high signal of interrupt prohibition is applied to the input of the OR gate, the OR gate output is forced to logic high, the voltage comparator output logic status is ignored.

5. Important Points

When the external amplifier is added to the system, the total gain is huge, the following points must be paid to special attention

1) The +5V and –5V voltage must be as symmetrical as possible, less than 5 mV is recommended.

2) Each power pin of U0 to U3 must have a pair of decoupling capacitors: 10uF (tantalum capacitor) parallel with 0.1 uF (ceramic capacitor).

3) A low pass filter R0 (10 k ohms to 100 k ohms) and C0 (o.1uF) should be inserted in the input of U0

4) During the huge gain, the voltage drift and 50/60 Hz noise would be difficult to be avoided, multiple A/D operations and average calculation are necessary

5) All resistor should be precise metal film type.